Doc. version :	1.2
Total pages :	25
Date :	2005.7.1

Product Specification

1.7″ COLOR TFT-LCD MODULE

MODEL NAME: A017CN01 V2

< ◆ > Preliminary Specification

< > Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0	25/Apr./2005		First draft,
1	15/Jun./2005	10; 25	Adds the description of register R1 and modify UPS052 timing.
		15	Update viewing angle
1.1	28/Jun./2005	18	Update packing format
1.2	1/Jul./2005	6	Update LED driving vlotage :Min 3.6, Typical 4.2,Max 4.6

Contents:

A. Physical specifications

NO.	Item	Specification	Remark
NO.	Item	Specification	Remark
1	Display resolution(dot)	480(W) ×240(H)	
2	Active area(mm)	34.08(W) ×25.56(H)	
3	Screen size(inch)	1.68(Diagonal)	
4	Dot pitch(mm)	0.071(W) ×0.1065(H)	
5	Color configuration	R. G. B. delta	
6	Overall dimension(mm)	41.58(W) ×37.26(H) ×2.8(D)	Note 1
7	Weight (g)	9	
8	Panel surface treatment	Hard coating (3H)	

Note 1: Refer to Fig. 4

B. Electrical specifications

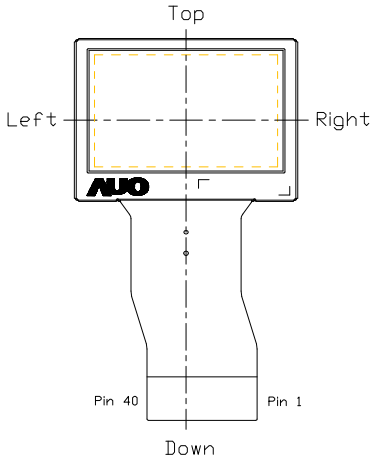
1.Pin assignment

Pin no	Symbol	I/O	Description	Remark
1	VCOM	I	Common electrode driving voltage	
2	Vgoff_H	PO	Negative high power supply for gate driver output: -12.5V+VCAC	
3	Vgoff_L	PO	Negative low power supply for gate driver output: -12.5V	
4	C4P	C	Pins to connect capacitance for power circuitry	
5	C4M	C	Pins to connect capacitance for power circuitry	
6	VGH	PO	Positive power supply for gate driver output: +12.5V	
7	FRP	O	Frame polarity output for VCOM	
8	VCAC	C	Define the amplitude of the VCOM swing	
9	Vint3	P	Intermediate voltage for charge Pump	
10	C3P	C	Pins to connect capacitance for power circuitry	
11	C3M	C	Pins to connect capacitance for power circuitry	
12	Vint2	P	Intermediate voltage for charge Pump	
13	C2P	C	Pins to connect capacitance for power circuitry	
14	C2M	C	Pins to connect capacitance for power circuitry	
15	Vint1	P	Intermediate voltage for charge Pump	
16	C1P	C	Pins to connect capacitance for power circuitry	
17	C1M	C	Pins to connect capacitance for power circuitry	
18	PGND	P	Charge Pump Power GND	
19	PVDD	P	Charge Pump Power VDD	
20	DRV	PO	Gate signal for the power transistor of the boost converter	
21	LED Anode	I	For Led Anode voltage	
22	GND	P	Digital GND	
23	FB	P	Main boost regulator feedback input	
24	AVDD	P	Analog power supply	
25	GND	P	Digital GND	
26	VCC	P	Digital power supply	
27	CS	I	Serial communication chip select	
28	SDA	I	Serial communication data input	
29	SCL	I	Serial communication clock input	
30	HSYNC	I	Horizontal sync input	
31	VSYNC	I	Vertical sync input	
32	DCLK	I	Clock Input:	
33	D7	I	Data Input: MSB	

34	D6	I	Data Input:	
35	D5	I	Data Input:	
36	D4	I	Data Input:	
37	D3	I	Data Input:	
38	D2	I	Data Input:	
39	D1	I	Data Input:	
40	D0	I	Data Input: LSB	

I: Input; O: Output. VI: voltage input VO: voltage output P:Power.

Note 1 : Definition of scanning direction. Refer to figure as below



2. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	V_{CC}	GND=0	-0.5	7.0	V	
	AV_{DD}	AV_{SS}=0	-0.5	7.0	V	
	PV_{DD}	PV_{SS}=0	-0.5	7.0	V	
Input signal voltage	VCOM	-	-2.9	5.2	V	
Operating temperature	Topa	-	-30	85	℃	Ambient temperature
Storage temperature	Tstg	-	-55	125	℃	Ambient temperature

3. Electrical characteristics

a. Typical operating conditions (GND=AVss=0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power Voltage		V_{CC}	2.7	3.0	3.6	V	
		PV_{DD},$AV_{DD,}$	3.0	3.3	3.6	V	
		VCDC	-0.1	0.1	0.3	V	
Output Signal voltage	H Level	V_{OH}	Vcc-0.4	-	VCC	V	
	L Level	V_{OL}	GND	-	GND+0.4	V	
Input Signal voltage	H Level	V_{IH}	0.7xV_{CC}	-	V_{CC}	V	
	L Level	V_{IL}	GND	-	0.3V_{CC}	V	
Output current	H Level	IOH	-	400	-	uA	
	L Level	IOL	-	-400	-	uA	
Analog stand by current		Ist	-	-	200	uA	DCLK is stopped

b. Current consumption (GND=AVss=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
-	Icc (Pin 25)	V_{CC}=3.3V	-	2	2.5	mA	-
-	I_{DD}	AV_{DD}=3.3V	1	1.5	2.0	mA	-

c. LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current			20	30	mA	
LED voltage	V_L	3.6	4.2	4.6	*V*	Note1
LED Life Time	L_L	10000			Hr	Note 2,3

Note 1 : Max.voltage :1pcs/4V, FB=0.6V, VL=LED anode(PIN 21)
Note 2 : Ta. = 25℃, I_L = 20mA
Note 3 : Brightness to be decreased to 50% of the initial value

4. AC Timing

a. Timing conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit.
Delay between Hsync and DCLK	Thc	-	-	1	DCLK
Hysnc width	Twh	1.0	-	-	DCLK
Hsync period	Th	60	63.56	67	us
Vsync setup time	Tvst	12	-	-	ns
Vsync hold time	Tvhd	12	-	-	ns
Hsync setup time	Thst	12	-	-	ns
Hsync hold time	Thhd	12	-	-	ns
Data set-up time	Tdsu	12	-	-	ns

Data hold time	Tdhd	12	-	-	Ns
Vsync to 1'th gate Output (No CCIR mode)	Tstv	6	13 (Note 1)	21	Th
First active video line to 1'th Gate Output for NTSC (CCIR Mode)	Tstv	11	18	26	Th
First active video line to 1'th Gate Output for PAL (CCIR Mode)	Tstv	17	24	32	Th
SD output stable time	Tst	-	-	30	us
GD output stable time	Tgst	-	500	1000	ns
Serial communication					
Serial clock period	Tsck	320	-	-	ns
Serial clock duty cycle	Tscw	40	50	60	%
Serial clock width	Tssw	120	-	-	ns
Serial data setup time	Tist	120	-	-	ns
Serial data hold time	Tihd	120	-	-	ns
CSB setup time	Tcst	120	-	-	ns
CSB data hold time	Tchd	120	-	-	ns
Chip select distinguish	Tcd	1	-	-	us
Delay between CSB and Vsync	Tcv	1	-	-	us

Note 1: The first valid data line on panel is G1=Tstv+1=14(Active area is 240 channels), please refer to Fig.14.

Note 2: Suggested frame rate >= 60HZ

b. Select data input format

SEL2	SEL1	SEL0	Data input format	Operating frequency
0	0	0	UPS051 path, special data format: DDX	9.7 MHz
0	0	1	UPS052 data format	24.54 MHz
0	1	0	UPS052 data format	27 MHz
0	1	1	YUV mode A data format	24.54 MHz
1	0	0	YUV mode A data format	27 MHz
1	0	1	YUV mode B data format	24.54 MHz
1	1	0	YUV mode B data format	27 MHz
1	1	1	CCIR 656 path, normal data format: DIN	27 MHz

c. Operating mode dependent AC characteristic

UPS051 Mode, SEL [2…0]=[000]

Parameter	Symbol	Min.	Typ.	Max.	Unit.
DCLK frequency	Fclk	*	9.7	-	Mhz
DCLK period	Tcph	-	10.3	-	ns

DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from Hsync to 1’st data input	Ths	84	100	115	DCLK
DC converter osc. Frequency	Fosc	-	303.1	-	khz

Note: It is suggested to keep frame rate more than 60HZ when using NTSC system.

d. Operating mode dependent AC characteristic

UPS052 or YUV Mode, SEL [2…0]=[001~110]

Parameter	Symbol	Min.	Typ.	Max.	Unit.
DCLK frequency	Fclk	-	24.54/27	-	Mhz
DCLK period	Tcph	-	40	-	ns
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from Hsync to 1’st data input	Ths	233	249	264	DCLK
DC converter osc. Frequency	Fosc	-	383.4/ 421.9	-	khz

e. Operating mode dependent AC characteristic

CCIR Mode, SEL [2…0]=[111]

Parameter	Symbol	Min.	Typ.	Max.	Unit.
DCLK frequency	Fclk	-	27	-	Mhz
DCLK period	Tcph	-	40	-	ns
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from Hsync to 1’st data input	Ths	257	273	288	DCLK
DC converter osc. Frequency	Fosc	-	421.9	-	khz

f. The configuration of serial data at SDA terminal is at below

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register address			X	DATA											

Register parameters

		Address			Content					
No.	Description	D15	D14	D13	D5	D4	D3	D2	D1	D0
R0	System setting	0	0	0	-	-	GRB	STB	SHDB	SHCB
R2	Driver Setting	0	1	0	-	-	-	-	U/D	SHL
R3	Timing setting	0	1	1	-	PALM	PAL	SEL2	SEL1	SEL0

R4	Data delay setting	1	0	0	-	DDL4	DDL3	DDL2	DDL1	DDL0
R5	Vertical delay setting	1	0	1	-	-	HDL3	HDL2	HDL1	HDL0
R6	VCAC level setting	1	1	0	-	-	-	VSCL2	VSCL1	VSCL0

Default register settings

		Address			Test	MSB											LSB
No.	Description	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	System setting	0	0	0	0	0	X	X	X	X	X	X	X	1	1	0	1
R2	Driver Setting	0	1	0	0	X	X	X	X	X	X	X	X	0	0	1	1
R3	Timing setting	0	1	1	0	X	X	X	X	X	X	X	0	0	0	0	1
R4	Data delay setting	1	0	0	0	X	X	X	X	X	X	X	0	0	0	0	0
R5	Vertical delay setting	1	0	1	0	X	X	X	X	X	X	0	0	0	0	0	0
R6	VCAC level setting	1	1	0	0	X	X	X	X	X	X	X	X	X	1	1	0

“X” => Don’t care.

Detail register function:

R0	GRB	I	Global reset pin (active low). GRB=”L”: The controller is resets, the charge pump and DCDC is off. GRB=”H”: Normal operation. **Default setting.**
R0	STB	I	Stand by mode (active low). STB=”L”: T_CON, source driver and DC-DC converter are off. All outputs are High-Z. STB=”H”: Normal operation. **Default setting.**
R0	SHDB	I	DC-DC converter shutdown signal (active low) SHDB=”L”: DC-DC converter is off. **Default setting.** SHDB=”H”: DC-DC converter is on.
R0	SHCB	I	Charge pump shutdown signal (active low). SHDB=”L”: Charge pump is off. SHDB=”H”: Charge pump is on. **Default setting.**
R2	U/D	I	Up/down scan control of gate driver. U/D=”L”: Scan up: First line=G240➔G239➔…➔G2➔Last line=G1. U/D=”H”: Scan down: First line=G1➔G2➔…➔G239➔Last line=G240. **Default setting.**
R2	SHL	I	Select left or right shift. SHL=”L”: Shift left: First data=S480➔S479➔…➔S2➔Last data=S1. SHL=”H”: Shift right: First data=S1➔S2➔…➔S479➔Last data=S480. **Default setting.**

<table>
<tr><td>R3</td><td>PAL</td><td>I</td><td>NTSC/PAL selection signal
PAL=”L”: Input data format is NTSC (240 active line). Default setting.
PAL=”H”: Input data format is PAL.</td></tr>
<tr><td>R3</td><td>PALM</td><td>I</td><td>PAL selection signal
PALM=”L”: Input data format is PAL 1/6,8(280 active line). Default setting.
PALM=”H”: Input data format is PAL 1/6(288 active line).
Only available when PAL=H.</td></tr>
<tr><td>R3</td><td>SEL [2…0]</td><td>I</td><td>Select input data format.
<table>
<tr><th>SEL2</th><th>SEL1</th><th>SEL0</th><th>Data input format</th><th>Operating frequency</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>UPS051 path, special data format: DDX</td><td>9.7 MHz</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>UPS052 data format</td><td>24.54 MHz</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>UPS052 data format</td><td>27 MHz</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>YUV mode A data format</td><td>24.54 MHz</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>YUV mode A data format</td><td>27 MHz</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>YUV mode B data format</td><td>24.54 MHz</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>YUV mode B data format</td><td>27 MHz</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>CCIR 656 path, normal data format: DIN</td><td>27 MHz</td></tr>
</table></td></tr>
<tr><td>R4</td><td>DDL [4…0]</td><td>I</td><td>Select the data delay timing.
<table>
<tr><th>DDL4</th><th>DDL3</th><th>DDL2</th><th>DDL1</th><th>DDL0</th><th>Delay</th><th>Unit</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Default</td><td rowspan="33">DCLK period</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>+1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>+2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>+3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>+4</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>+5</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>+6</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>+7</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>+8</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>+9</td></tr>
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<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>+15</td></tr>
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<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>-2</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>-3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>-4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>-5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>-6</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>-7</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>-8</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>-9</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>-10</td></tr>
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<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>-16</td></tr>
</table></td></tr>
</table>

<table>
<tr>
<td>R5</td>
<td>HDL [3…0]</td>
<td>I</td>
<td>Select the first active line delay timing.
<table>
<tr><th>HDL3</th><th>HDL2</th><th>HDL1</th><th>HDL0</th><th>Delay</th><th>Unit</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Default</td><td rowspan="17">Hsync period</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>+1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>+2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>+3</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>+4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>+5</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>+6</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>+7</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>+8</td></tr>
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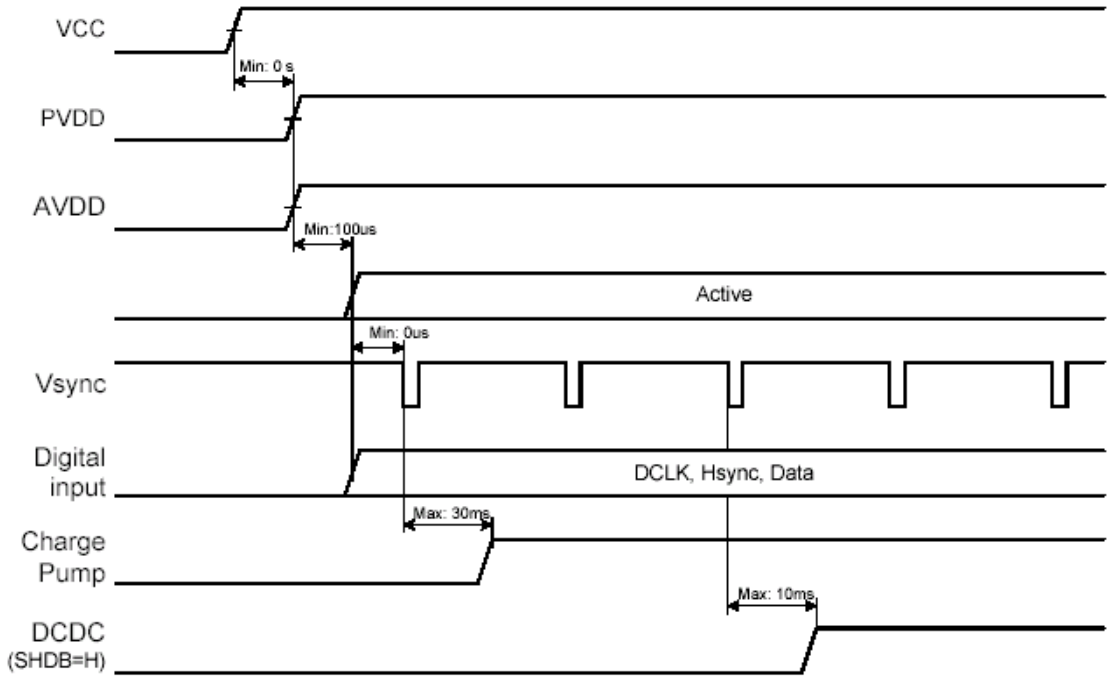
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>-2</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>-3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>-4</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>-5</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>-6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>-7</td></tr>
</table>
</td>
</tr>
<tr>
<td>R6</td>
<td>VCSL [2...0]</td>
<td>I</td>
<td>VCAC voltage selection
VCSL Default setting: 110
<table>
<tr><th>VCSL</th><th>VCAC[V]</th></tr>
<tr><td>010</td><td>5</td></tr>
<tr><td>011</td><td>5.2</td></tr>
<tr><td>100</td><td>5.4</td></tr>
<tr><td>101</td><td>5.6</td></tr>
<tr><td>110</td><td>5.8</td></tr>
<tr><td>111</td><td>6</td></tr>
<tr><td>000</td><td>6.2</td></tr>
<tr><td>001</td><td>6.4</td></tr>
</table>
</td>
</tr>
</table>

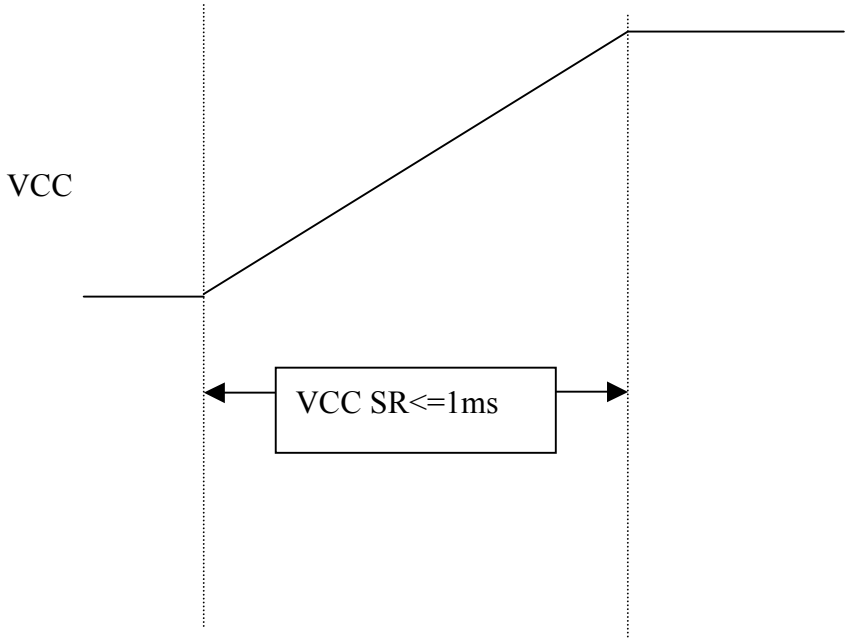
g. Power on sequence and VCC slew rate specification.

1. Suggested Power on sequence with Panel Power input and Data.

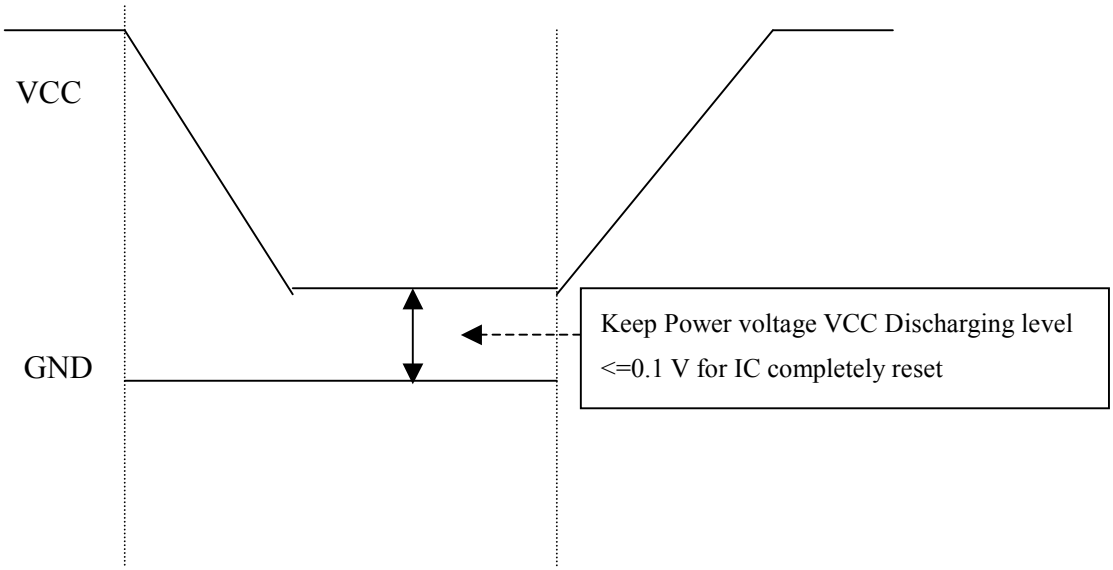


Note: Vsync, Hsync, and data should be active after VCC enable to eliminate leakage.

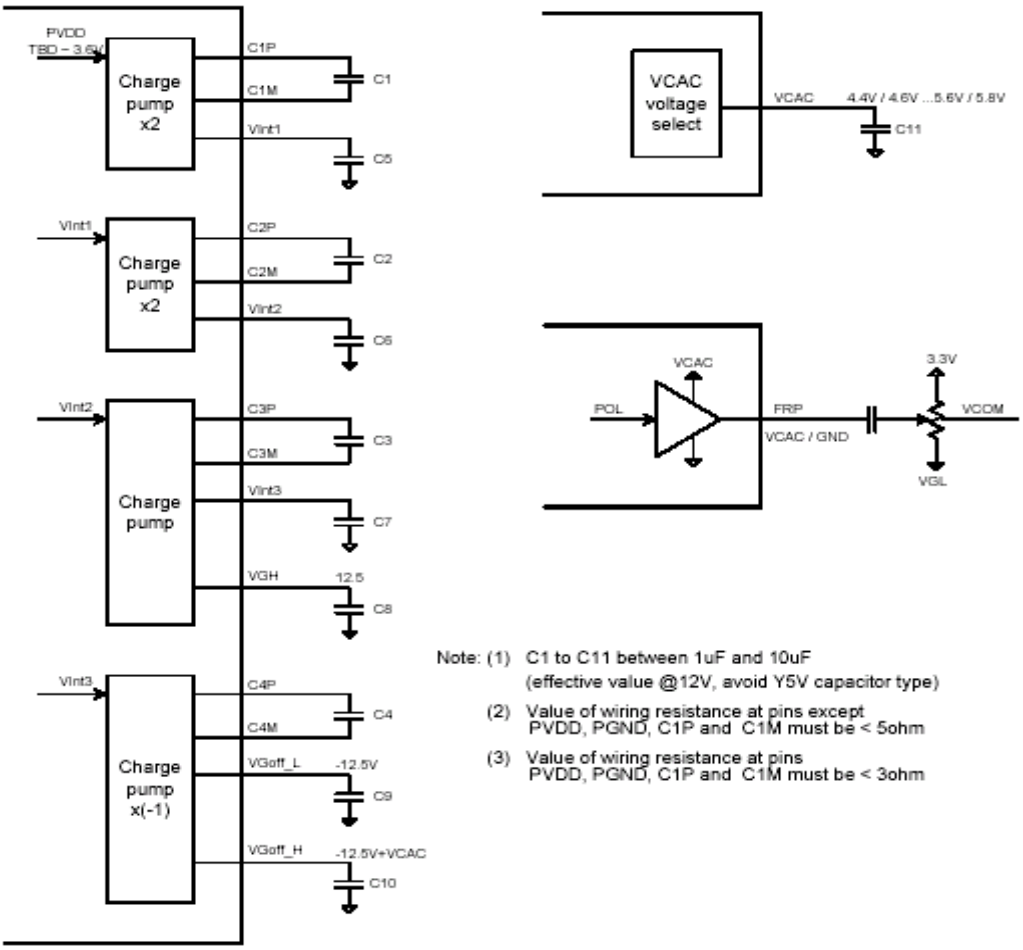
2. Suggested VCC Slew rate is below 1ms.



3. Suggested VCC discharging voltage<=0.1V.



Charge pump Application circuit

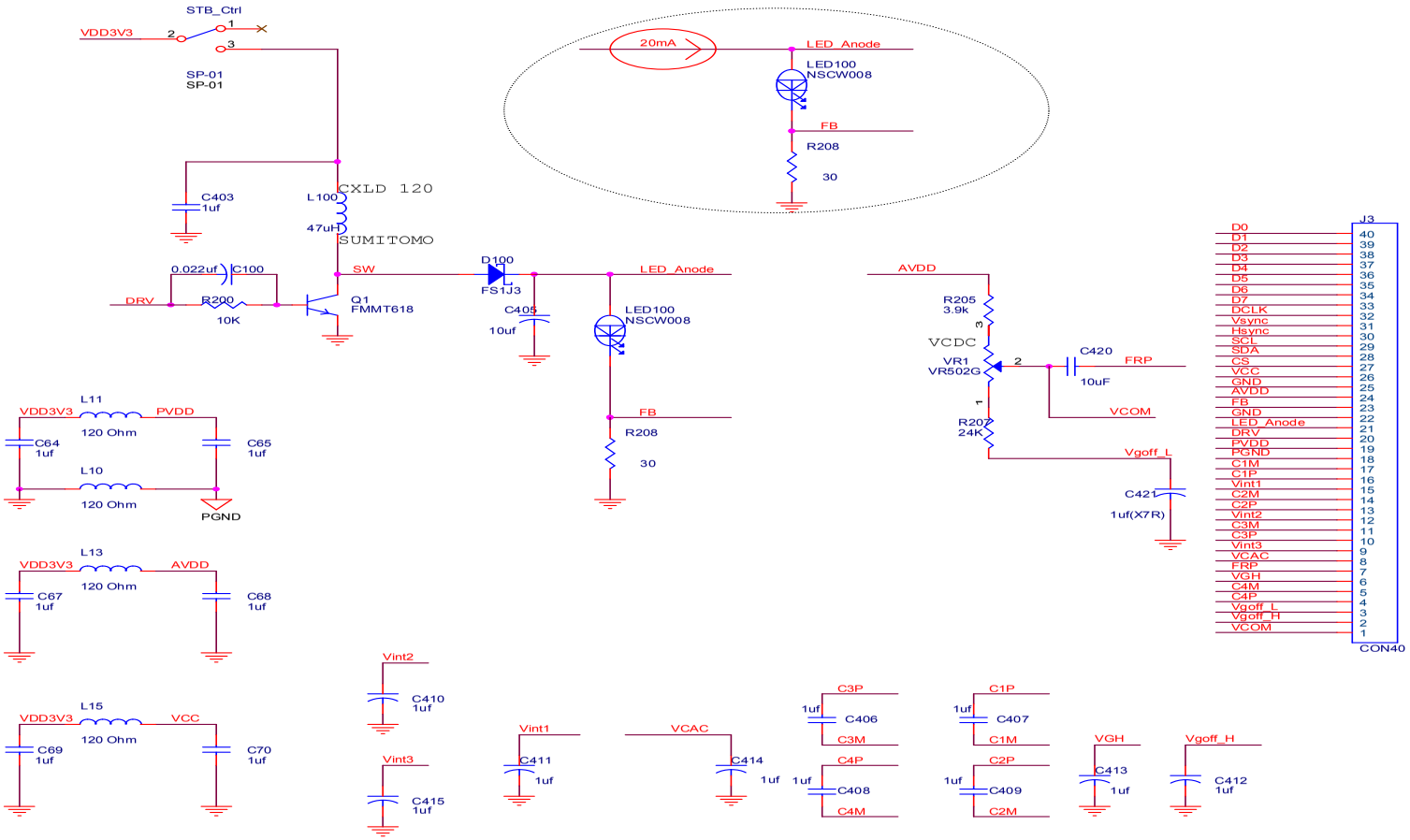


Note: (1) C1 to C11 between 1uF and 10uF
(effective value @12V, avoid Y5V capacitor type)

(2) Value of wiring resistance at pins except PVDD, PGND, C1P and C1M must be < 5ohm

(3) Value of wiring resistance at pins PVDD, PGND, C1P and C1M must be < 3ohm

5. Reference Circuit


STB_Ctrl
VDD3V3
SP-01
SP-01
C403
1uf
L100
CXLD 120
47uH
SUMITOMO
0.022uf
C100
DRV
R200
10K
Q1
FMMT618
SW
D100
FS1J3
C405
10uf
LED_Anode
LED100
NSCW008
FB
R208
30
20mA
AVDD
R205
3.9k
VCDC
VR1
VR502G
C420
10uF
FRP
VCOM
R207
24K
Vgoff_L
C421
1uf(X7R)
L11
VDD3V3
PVDD
120 Ohm
C64
1uf
C65
1uf
L10
120 Ohm
PGND
L13
VDD3V3
AVDD
120 Ohm
C67
1uf
C68
1uf
L15
VDD3V3
VCC
120 Ohm
C69
1uf
C70
1uf
Vint2
C410
1uf
Vint3
C415
1uf
Vint1
C411
1uf
VCAC
C414
1uf
C3P
C406
C3M
C4P
C408
C4M
C1P
C407
C1M
C2P
C409
C2M
VGH
C413
1uf
Vgoff_H
C412
1uf
J3
D0
D1
D2
D3
D4
D5
D6
D7
DCLK
Vsync
Hsync
SCL
SDA
CS
VCC
GND
AVDD
FB
GND
LED_Anode
DRV
PVDD
PGND
C1M
C1P
Vint1
C2M
C2P
Vint2
C3M
C3P
Vint3
VCAC
FRP
VGH
C4M
C4P
Vgoff_L
Vgoff_H
VCOM
CON40

C. Optical specification (Note 1,Note 2, Note 3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time Rise Fall	 Tr Tf	 θ =0°	 - -	 25 30	 50 60	 ms ms	Note 4
Contrast ratio	CR	At optimized viewing angle	120	300	-		Note 5,6
Viewing angle Top Bottom Left Right		CR≧10	 10 30 40 40	 15 35 45 45	 - - - -	deg.	Note 7
Brightness	Y_L	θ =0°	100	180	-	cd/m^2	Note 8
White chromaticity	x	θ =0°	(0.26)	(0.31)	(0.36)		
	y	θ =0°	(0.28)	(0.33)	(0.38)		

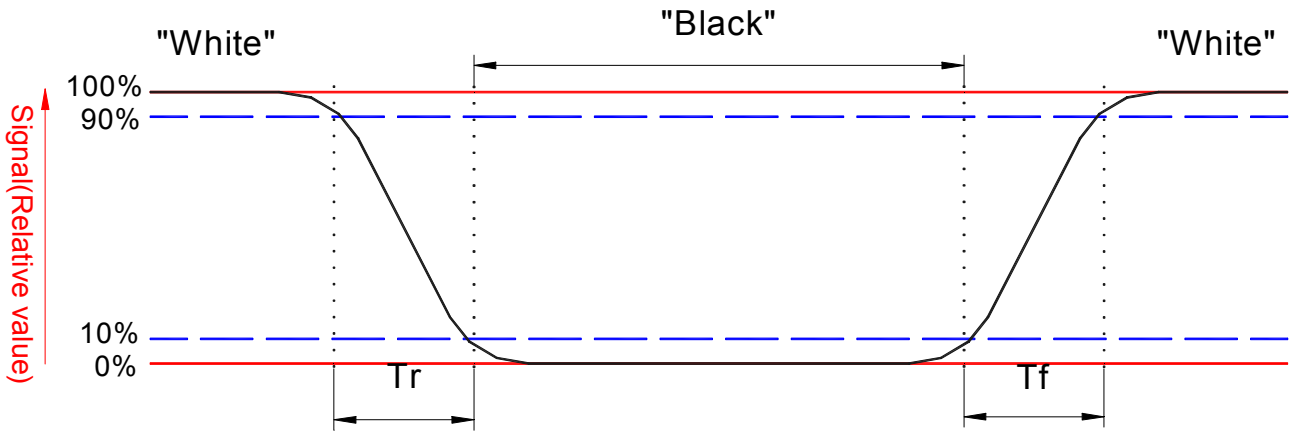
Note 1. Ambient temperature =25℃.

Note 2. To be measured in the dark room.

Note 3.To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation.

Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6. White $Vi=V_{i50} \mp 1.5V$

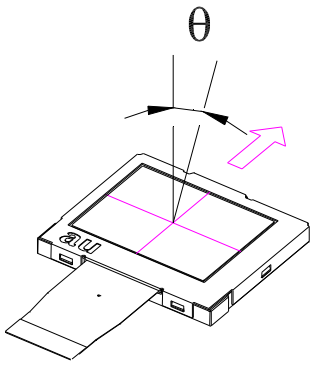
Black $Vi=V_{i50} \pm 2.0V$

“±” Means that the analog input signal swings in phase with COM signal.

“∓” Means that the analog input signal swings out of phase with COM signal.

V_{i50} : The analog input voltage when transmission is 50%
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle:
Refer to figure as below.



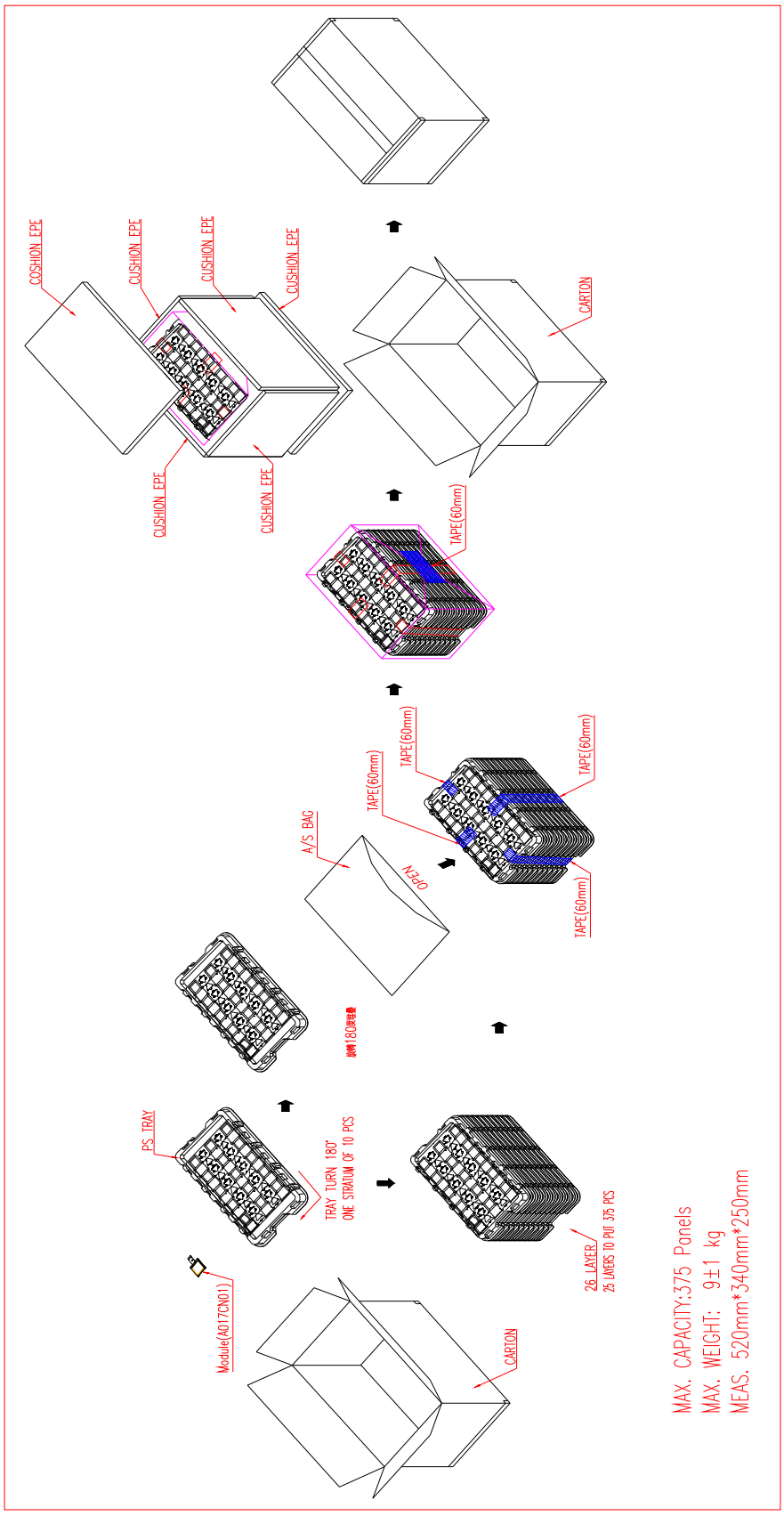
Note 8. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

D. Reliability test items:

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 80℃ 240Hrs	
2	Low temperature storage	Ta= -25℃ 240Hrs	
3	High temperature operation	Ta= 60℃ 240Hrs	
4	Low temperature operation	Ta= 0℃ 240Hrs	
5	High temperature and high humidity	Ta= 60℃. 90% RH 240Hrs	Operation
6	Heat shock	-25℃~80℃/50 cycle 2Hrs/cycle	Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω), once for each terminal	Non-operation
8	Vibration (with carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
9	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note: Ta: Ambient temperature.

E. Packing form



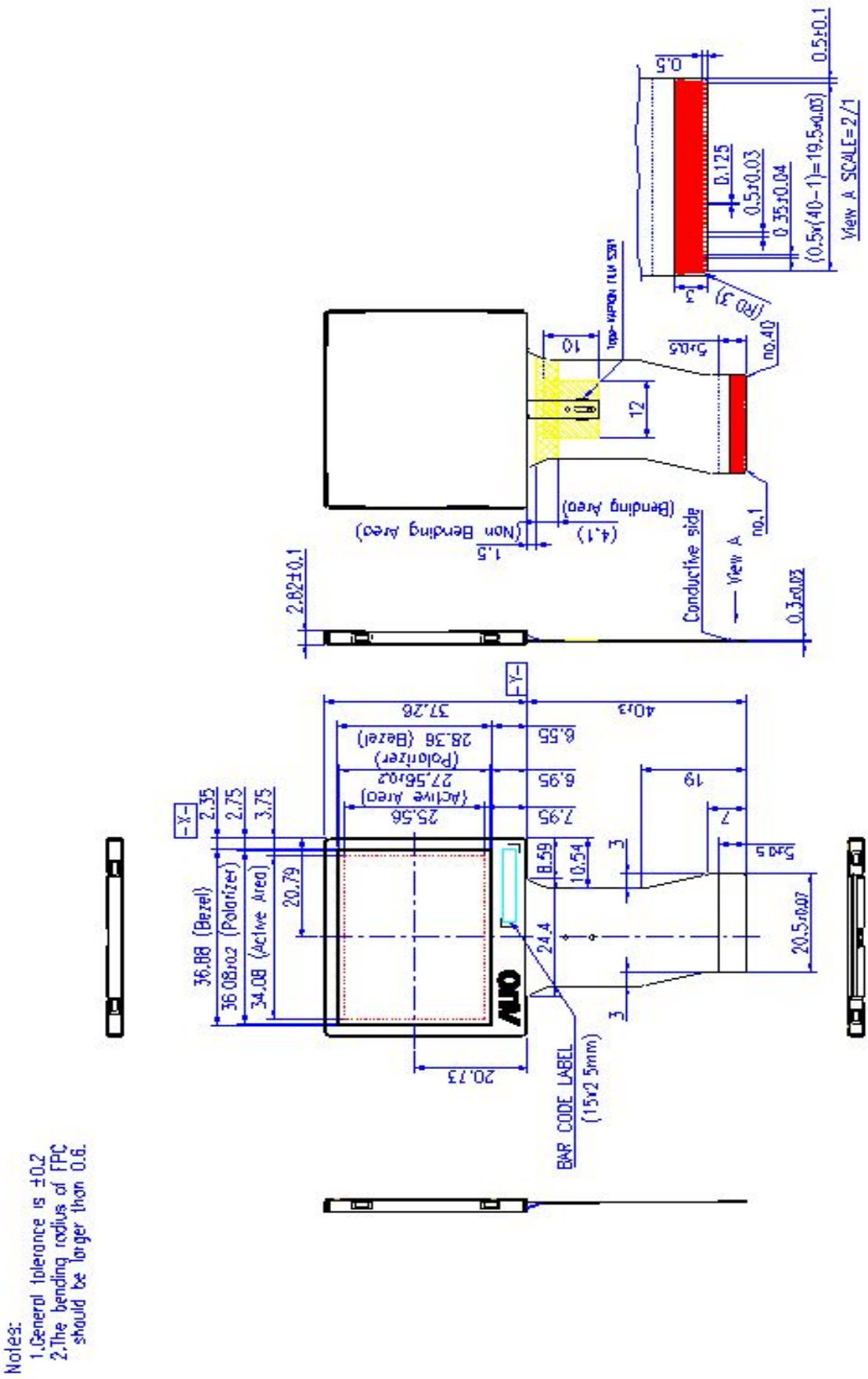


Fig. 4 Outline dimension of TFT-LCD module

F. Timing format

Serial communication timing

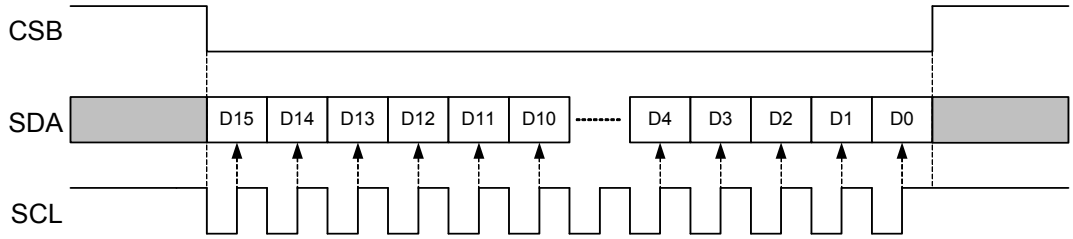


Figure 1: Serial communication diagram

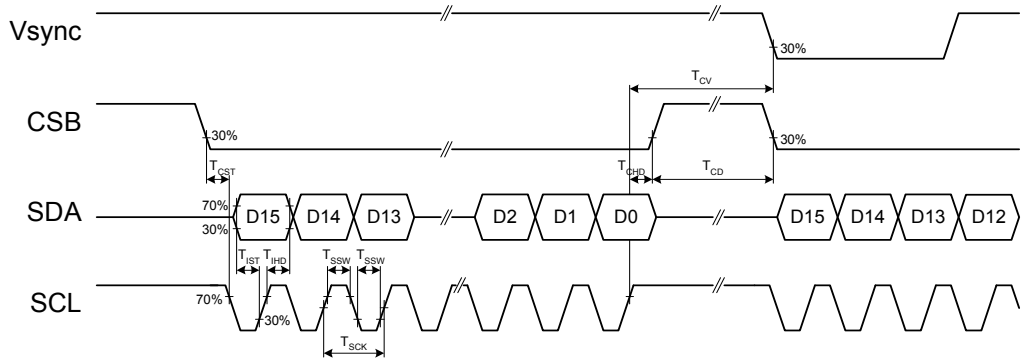


Figure 2: Serial communication timing

Stand-by timing

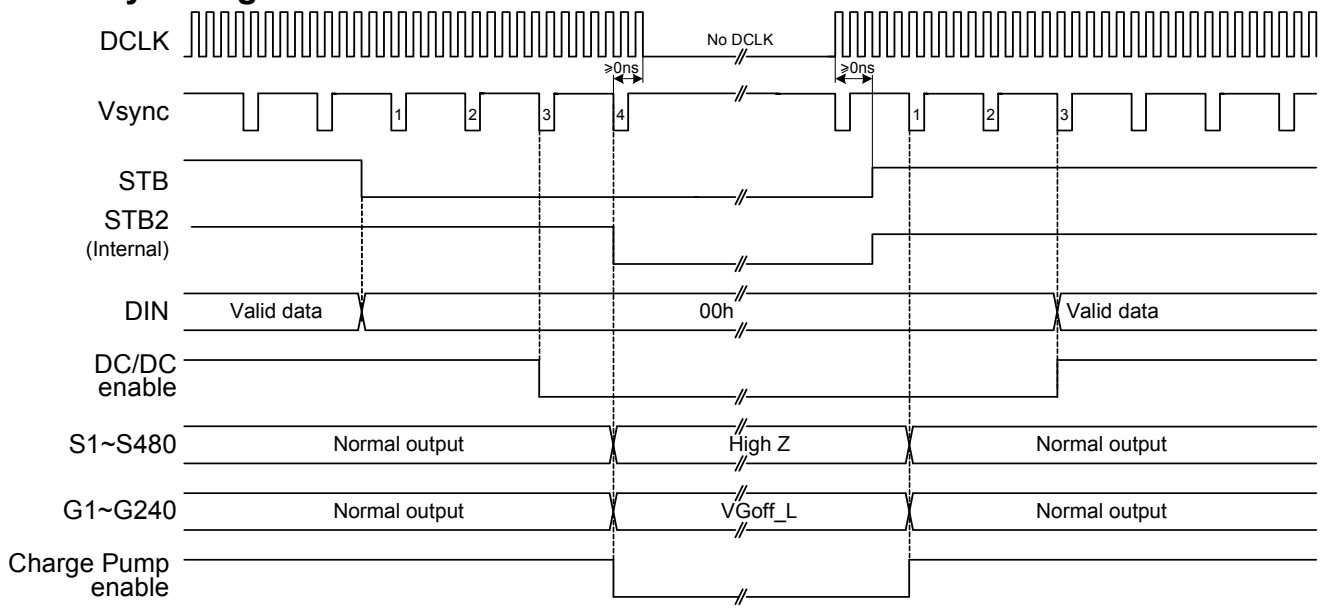


Figure 3: Stand-by timing diagram

UPS051 timing

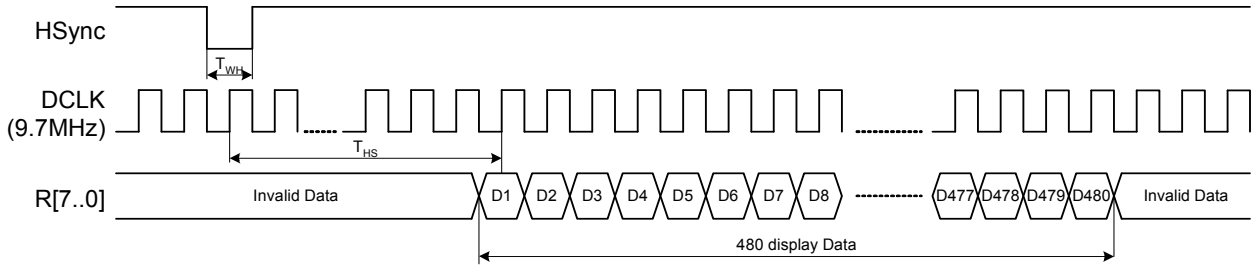


Figure 4: UPS051 Data sampling timing

UPS052 timing

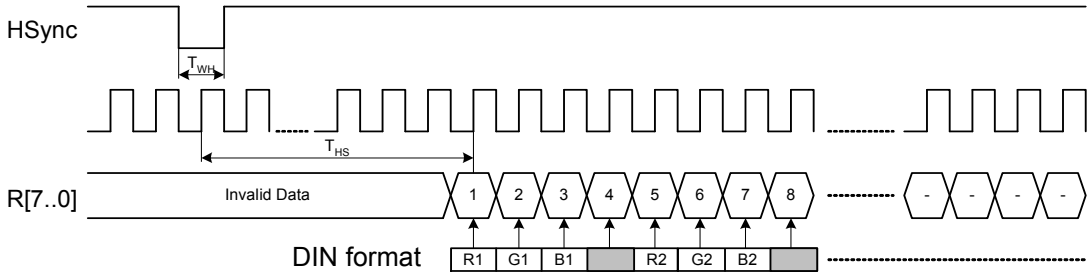


Figure 5: UPS052 Data sampling

UPS052 24.54MHz timing

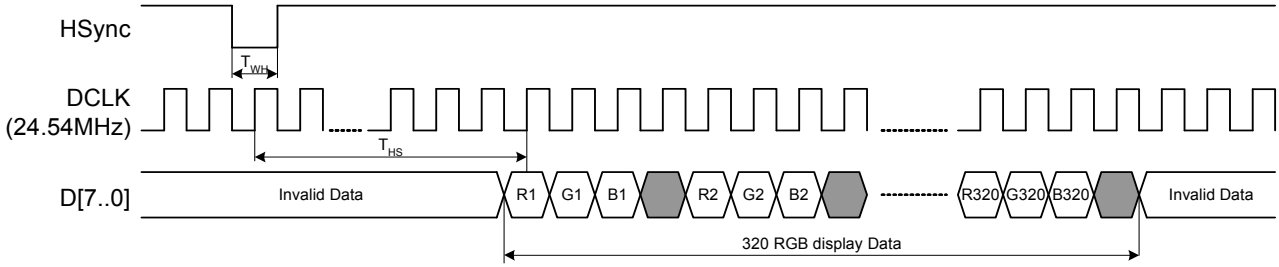


Figure 6: UPS052 24.54 MHZ Data sampling

UPS052 27MHz timing

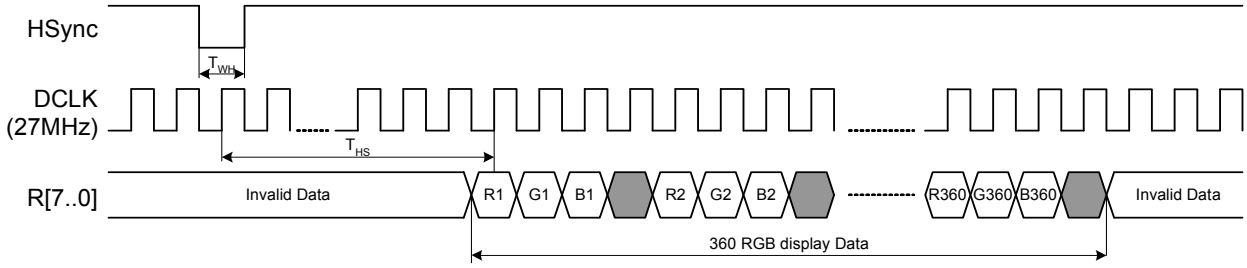


Figure 7: UPS052 27 MHZ Data sampling

YUV timing

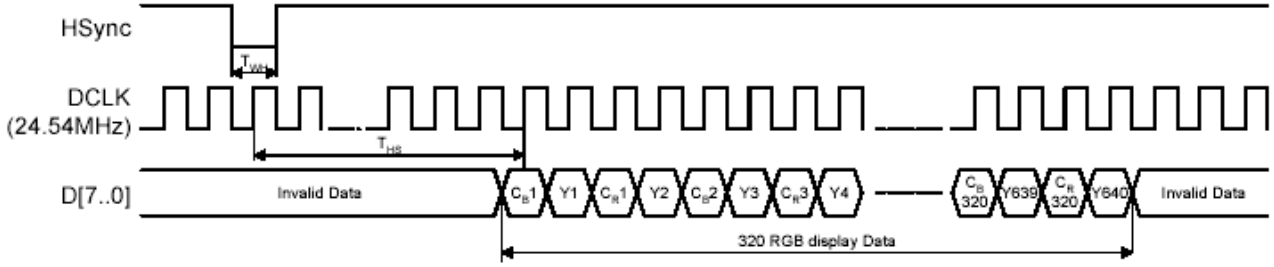


Figure 8: YUV mode A 24.54MHz Data input format

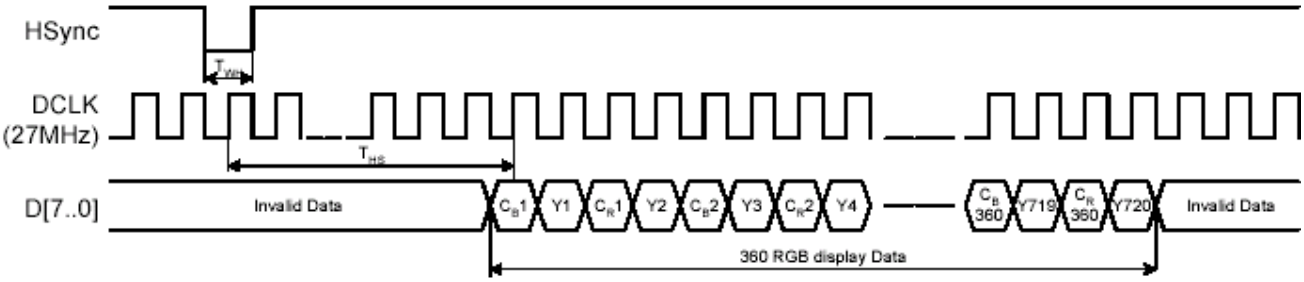


Figure 9: YUV mode A 27MHz Data input format

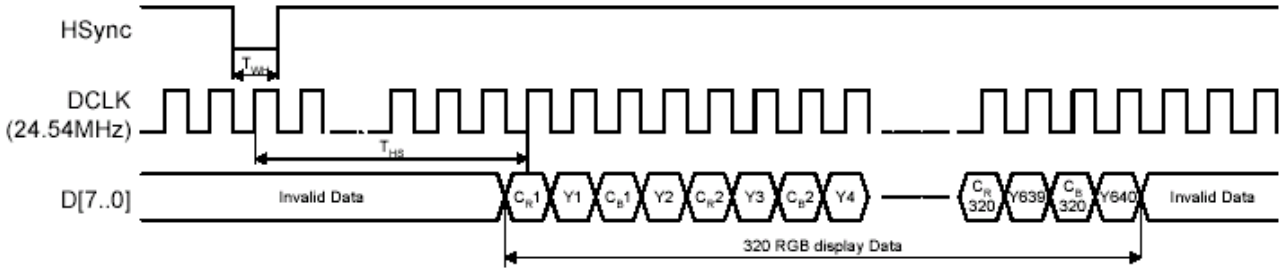


Figure 10: YUV mode B 24.54MHz Data input format

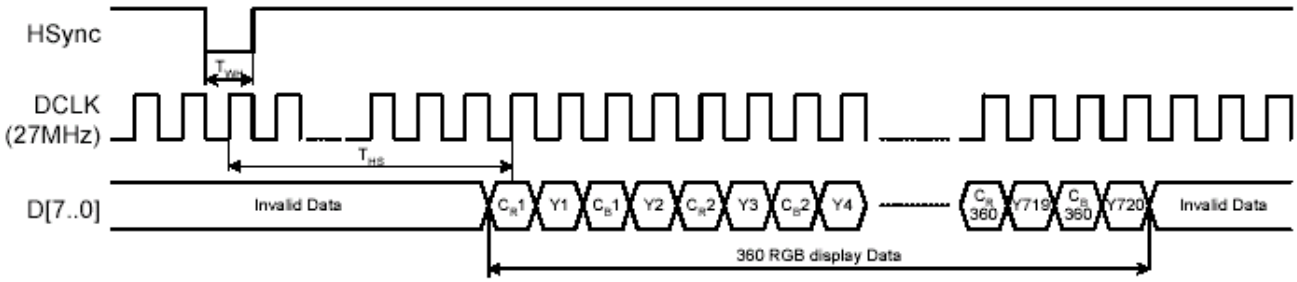


Figure 11: YUV mode B 27MHz Data input format

CCIR 656 timing

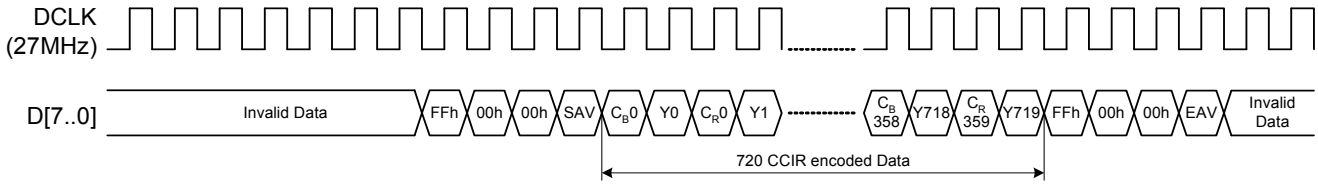


Figure 12: CCIR Data input format

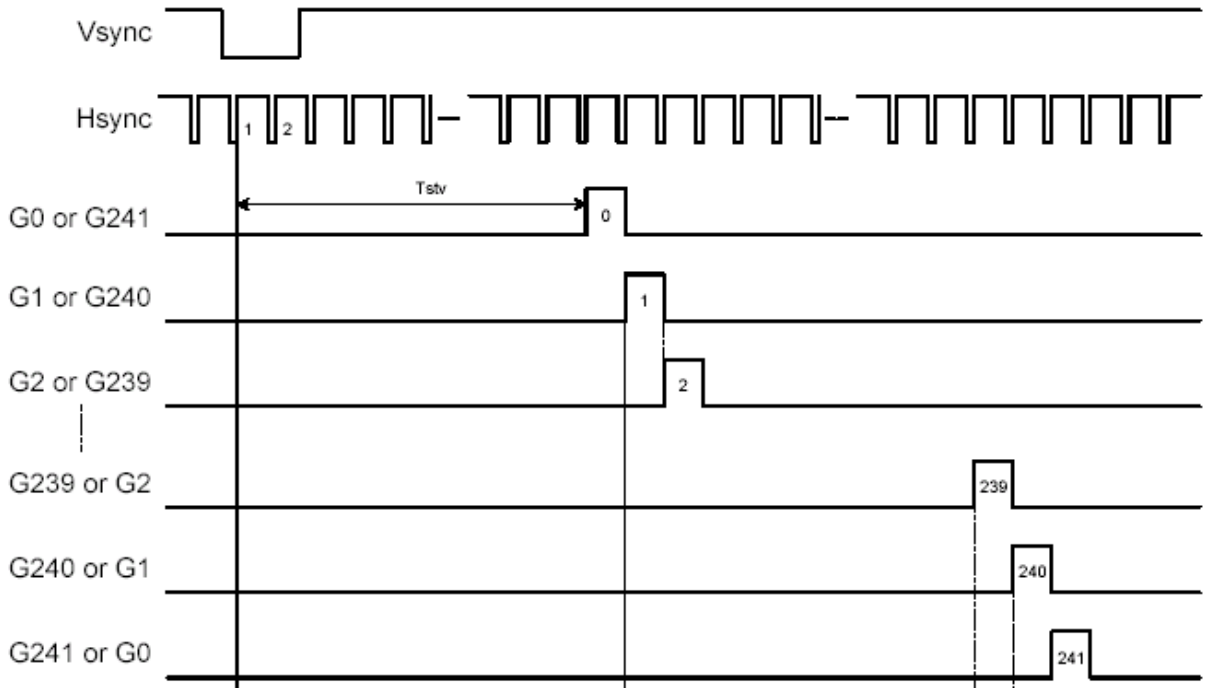


Figure 13: Vertical timing diagram

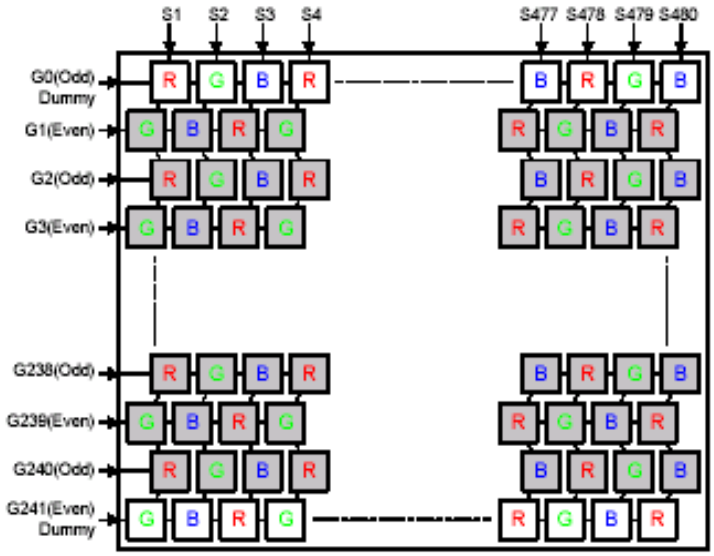


Figure 14: Delta pixel arrangement